REMARKS

Claims 1 - 21 are pending, of which claims 17 - 20 have been withdrawn from consideration. By this Amendment, claims 1, 2 and 21 have been amended. The applicants respectfully submit that no new matter has been added. It is believed that this Response is fully responsive to the Office Action dated September 14, 2000.

35 U.S.C. §112, Second Paragraph, Rejection:

In item 3 of the Office Action, claims 2 and 3 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regards as their invention.

This rejection is respectfully traversed.

Applicants respectfully submit that the amendments to claim 2 obviates the rejection of claims 2 and 3 under 35 U.S.C. §112, second paragraph. Accordingly, withdrawal of the rejection of claims 2 and 3 under 35 U.S.C. §112, second paragraph, is respectfully solicited.

As To The Merits:

As to the merits of this case, the Examiner sets forth the following rejections:

(1) claims 1-16 and 21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over **Mochizuki et al.** (of record) in view of **Ochiai** (of record) or **Watanabe et al.** (of record); and

(2) claims 1-13, 16 and 21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over **Ochiai** or **Watanabe et al.** taken with **Zafar** (of record) in view of **Kawai et al.** (of record) and **Yamazaki et al.** (of record).

These rejections are respectfully traversed.

Significant structural arrangements of the applicants' claimed invention, as amended, now includes forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a range which passes through the first opening and the second opening.

None of the applied references, singly or in combination, teach or fairly suggest the significant structural arrangements of the applicants' claim invention concerning forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a range which passes through the first opening and the second opening.

The applied reference of **Mochizuki** discloses, as shown in FIG. 12, forming: an impurity diffusion layer(n/s) in a semiconductor substrate, a first insulation film 13; a first opening on the impurity diffusion layer; a plug by embedding a refractory metal to the opening on the impurity diffusion by a metal CVD method; a lower electrode 17, an oxide dielectric film 18 and an upper electrode 19 as a capacitor on the first insulating film; a second insulating film 20; a second opening on an upper portion of the plug and the upper electrode; a local interconnection for connecting the plug on the diffusion layer and the upper electrode; and a third insulating film 23.

Mochizuki's purpose is to prevent deterioration of a polarization-characterization. **Mochizuki** has the problem that when an interconnection is formed by a metal CVD method or MO-CVD method which has a good step coverage after the oxide dielectric film is formed, a characterization of a capacitor is deteriorated by a diffusion of hydrogen which is a reduction gas.

In order to solve this problem, **Mochizuki** performs the steps of forming the flattened first insulating, forming the opening on the diffusion layer embedded the refactory metal to the opening and forming plug.

Since an under interlayer is formed flatly, an interconnection can be formed on a capacitor by a sputtering method and not by using a reduction gas such as hydrogen. In this matter, it can prevent deterioration of a capacitor characterization.

Mochizuki does not disclose the steps of forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film as set forth in amended claims 1 and 21.

The interconnection 22 is formed outside the upper electrode in sectional views Fig. 21, etc. of **Mochizuki**, but the interconnection layer 22 is formed inside the upper electrode in Fig.8. In addition, while **Mochizuki** may disclose a TiN film as an interconnection, it is not described that the TiN film is a blocking layer for preventing a diffusion of hydrogen.

The applied reference of **Ochiai** discloses, as shown in Figs.1 to 4 forming: a impurity diffusion layer 8; a first insulation film 62; a lower electrode 31, an oxide dielectric film 2 and an upper electrode 32 as a capacitor; a second insulating layer 63; an opening on the impurity layer,

embedding a diffusion preventing film to the opening layer, annealing for decreasing a contact resistance, removing the diffusion preventing film; an opening on the upper electrode; and an interconection11 for connecting the opening and the upper electrode.

In other words, a purpose of **Ochiai** is to prevent a diffusion of an impurity which causes a junction leak of a transistor from an oxide dielectric film consisting of PZT, etc. in the step of the annealing for decreasing a contract resistance.

Ochiai does not disclose the step of forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contact with the oxide dielectric film as recited in amended claims 1 and 21.

That is, an edge of the interconnection 11 is clearly formed inside of the upper electrode 32 in Fig.4 of **Ochiai**.

With regard to **Watanabe**, a step similar to **Ochiai** is disclosed by **Watanabe**. That is, the purpose of **Watanabe** is to prevent peeling between an oxide dielectric film and a lower electrode by diffusion of a reduction gas to a capacitor.

For this reason, a metal nitride film 13, as a cap film, is directly formed on an upper electrode of a capacitor. However, the metal nitride film 13 is directly formed with the same area to the upper electrode of a capacitor.

In contrast, in amended claims 1 and 21, an interconnection is formed with covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contact with the oxide dielectric film.

Accordingly, the advantage of preventing diffusion of reduction gas into a capacitor is greater in the present claimed invention than in **Watanabe**. Moreover, an interconnection, as shown in Figs.1 to 9 of **Watanabe**, is formed with a smaller area than an area where an upper electrode contacts with an oxide dielectric film.

The applied reference of **Zafer** discloses forming: an impurity diffusion layer 204 in a semiconductor substrate 20; a first insulating film 22 on the semiconductor substrate 20; a lower electrode 242, an oxide dielectric film 244 and an upper electrode 246 as a capacitor; a second insulating film 32 on the capacitor; an opening on the impurity diffusion layer of the upper electrode; an interconnection for connecting the diffusion layer and the upper electrode; and a third insulating firm 524.

The purpose of **Zafer** is to prevent degradation of a polarization-characterization of a dielectric film. For this reason, stress of a second insulating and a third insulating film is controlled so as to make to total the stress of the second insulating and the third insulating film small.

In other words, **Zafer's** purpose is completely different from that of the present claimed invention. Moreover, **Zafer** does not disclose the step of forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film. That is, an edge of an interconnection, as shown in Figs.4 and 5 of **Zafer**, is clearly formed inside a region where an upper electrode contacts with a dielectric film.

The applied reference of **Kawai** discloses forming: an impurity diffusion layer 26, 26d and a salicie layer 29 in a semiconductor substrate 1; a first insulating film 30; a lower electrode 31, an oxide dielectric film 32 and an upper electrode 33 as a capacitor; a second insulating film 34 on the capacitor; an opening 36 to 36g on the impurity diffusion layer the upper electrode; an interconnection 37a to 37s for connecting the diffusion layer and the upper electrode; and a third insulation film.

The purpose of **Kawai** is to prevent oxidation of the impurity diffusion layer in the step of annealing with oxygen to recover a deterioration of the oxide dielectric film after the opening of the impurity diffusion layer and the upper electrode. Therefore,the oxidation of the impurity diffusion layer is prevented by the salicide on the impurity diffusion layer.

However, **Kawai** does not disclose forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contact with the oxide dielectric film as now set forth in amended claims 1 and 21.

That is, the interconnection layer 37a, in Fig.2H of **Kawai**, is formed on an area which is larger than an area where the upper electrode contact with the oxide dielectric film accidentally. Since a plan view of the interconnection and the upper electrode is not disclosed and the purpose of the present claimed invention claim 1 is not described, the interconnection layer 37a, in Fig.2H does not disclose or fairly suggest the features set forth in amended claims 1 and 21.

Thus, for at least these reasons, it is respectfully asserted that the prior art fails to teach or suggest recitations of claims 1-16 and 21, and request that the Examiner allow these claims, along with the entire application, to issue. Accordingly, withdrawal of the rejection of claims 1-16 and 21 under 35 U.S.C. §103(a) is respectfully solicited.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment.

IN THE CLAIMS:

Please amend claims 1, 2 and 21 as follows:

1. (Amended) A method of manufacturing a semiconductor device comprising the steps of :

forming an impurity diffusion layer in a semiconductor substrate;

forming a first insulating film covering the semiconductor substrate;

forming a lower electrode of a capacitor on the first insulating film;

forming an oxide dielectric film of the capacitor on the lower electrode;

forming an upper electrode of the capacitor on the oxide dielectric film;

forming a second insulating film for covering the capacitor;

forming a first opening which exposes the impurity diffusion layer and a second opening which exposes the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film;

forming a metal film on the second insulating film for connecting electrically the impurity diffusion layer via the first opening and the upper electrode via the second opening;

forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area [in a range which passes through the first opening and the second opening and contains at least a region] where the upper electrode contacts with the oxide dielectric film, in a range which passes through the first opening and the second opening, by patterning the metal film; and

forming a third insulating film for covering the local interconnection.

Claim 2, line 2 delete "the" and substitute therefore --an--.

21. (Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming an impurity diffusion layer in a semiconductor substrate;

forming a first insulating film covering the semiconductor substrate;

forming a lower electrode of a capacitor on the first insulating film;

forming an oxide dielectric film of the capacitor on the lower electrode;

forming an upper electrode of the capacitor on the oxide dielectric film;

forming a second insulating film for covering the capacitor;

forming a first opening which exposes the impurity diffusion layer and a second opening which exposes the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film;

forming a metal film on the second insulating film for connecting electrically the impurity diffusion layer via the first opening and the upper electrode via the second opening;

forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area [in a range which passes through the first opening and the second opening and contains at least a region] where the upper electrode contacts with the oxide dielectric film, in a range which passes through the first opening and the second opening, by patterning the metal film, wherein the local interconnection is a blocking layer for preventing a diffusion of a redundant to the oxide dielectric film; and

forming a third insulating film for covering the local interconnection.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON

Thomas E. Brown
Attorney for Applicants
Reg. No. 44,450

Atty. Docket No. **990535**
1725 K Street, N.W., Suite 1000
Washington, DC 20006
Tel: (202) 659-2930
Fax: (202) 887-0357
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